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Modified Efficient OMS LUT Design for Memory-Based Multiplication

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Abstract: ***This paper proposes an efficient LUT (Look-Up-Table) design called Efficient EOMS (Efficient-OMS Design) for memory-based operations. This proposed design can be used for FPGA implementation as well as ASIC. The proposed design is a better choice than ordinary OMS (Odd Multiplier Store) and is preferred in many DSP calculations where one of the inputs to the filter coefficients is fixed. In this design (N+1), the possible product terms of the input multiplicands with fixed coefficients are stored directly in memory. Doing so allows for a simpler and faster design, unlike the previous proposal OMS (Odd Multiple Storage).Designs that extract odd multiples of the product term can significantly reduce path delay and area complexity with very simple control circuitry. Using (N+1) technology can significantly reduce the area compared to ordinary OMS technology. Additionally, the EOMS technical design is coded in Verilog and simulated and synthesized using Xilinx tools.***

Keywords: Digital Signal Processing, VLSI, FIR Filter, Memory-Based Computations, LUT.

1. INTRODUCTION

With the use of progressive scaling of the devices the semiconductor memory has become more power-efficient, cheaper and faster. In addition, the Global Semiconductor Innovation Guide predicts that embedded memory will be overwhelmingly close to the chip architecture and may account for more than 90% of the total SOC content [1-2]. Furthermore, the transistors that drive the density of memory segments not only scale faster than the density of reasonable parts, but were discovered [3].Furthermore, memory-based computational structures are more general than replicated population structures and offer different preferences. Memory-based computing architectures are suitable for many applications related to digital signal processing (DSP), a key component of the digital revolution sweeping

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the human world [5]. It seems to work with almost all automation and programmable devices. The DSP algorithms used in the system usually require extensive computer-based calculations in real-time situations [6]. Furthermore, DSP systems exist in portable and compact systems that operate on limited battery power, requiring these systems to occupy less silicon area [7]. Therefore, DSP system design is demanding, constrained by the following requirements: smaller area complexity, lower power consumption and faster operation. It is impossible to design a system that satisfies all application constraints [8]. Architectural transformations can be performed to trade off one constraint against another, such as the speed domain. Concrete solutions that help reduce the arithmetic complexity of the algorithm can be found in [9] to address speed, area, and power complexity.

All in all, multipliers are the essential segments of cryptography frameworks like elliptic bend cryptography calculations and advanced sign handling calculations like quick Fourier change (FFT) [10]. The multipliers are a fundamental piece of increase aggregate circuit (MAC), which is the core of advanced sign processor, where two information operands are duplicated and the present augmentation result is added to the past MAC result [11]. Any advanced channel application like Finite Impulse Response (FIR) requires a multiplier to play out the activity. The multiplier with lesser profundity, lower control necessity and lower zone sway the computerized framework to accomplish elite number juggling accomplish superior arithmetic [12].

Studies have shown that multiplier implementations for DSP applications fall into three categories: CORDIC implementations, adder-based implementations, and memory-based implementations [13]. Of the three, memory-based implementations are gaining popularity due to the significant growth of VLSI memory technology.Semiconductor memory is becoming cheaper, faster and consumes less power due to continuous improvements in silicon scaling technology. Advances in memory technology [14-18] have enabled better memory design based on application requirements today, and efficient memory-based multipliers are also possible.In the past, memory was a separate part of the processor unit, but now memory is part of the processor [19-22]. Since OMS-based multipliers already exist, I wanted to try an efficient OMS-based multiplier design that I hadn't explored and dealt with before. We were able to achieve a design with very low data path latency compared to previous designs.Although this work is incremental to the work of [24-28], it is new, and our proposed efficient OMS multiplier is an area-efficient and fast design compared to previous OMS designs.

Conventional Memory-Based Multiplier

Traditional memory-based multipliers are used for memory-based calculations and applied to fixed coefficients. In this design, all product terms are stored in memory specifying unsigned inputs. Suppose M is the word length of the fixed coefficient S and N is the word length of the input multiplicand Y.The number of memory locations it occupies is based on the length of Y. For example, for a 4-bit input, a total of 16 memory locations are occupied. Hence, we can say that for N-bit input a total of 2^N memory locations. Table 1 shows the contents of memory for N=4 and for fixed coefficient P. Fig.1, shows the principle involved in LUT - based multiplier.

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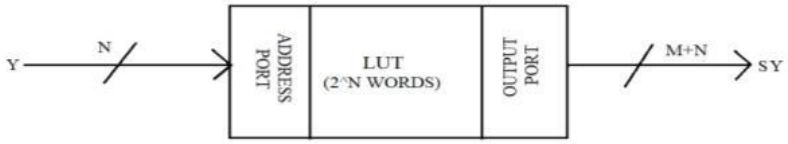

Fig 1: Basic of Memory-Based Computation

Proposed LUT-based Efficient OMS based multiplier for VLSI-DSP Computations:
Various techniques in the past have been devised for memory-based computations of LUT-based multiplier. In this section, an area-efficient technique is proposed, which is an Efficient OMS technique for 4-bit input. In this optimization for LUT from the odd multiples only (N+1) odd multiples are stored in memory which is [0001],[0101],[1001],[1101] and [1111] are stored in memory rest multiples can be obtained by right shift operation as shown in Table 2. The right shift operation is achieved by the use of appropriate barrel shifter which reduces the memory storage in comparison to the conventional technique. Table 1 depicts the basic truth-table for the 4-bit multiplication which shows the storage scheme for the odd multiples in the memory in which rest terms are obtained by right shifting of the bits. Address Y = (0000) provides product value (S.X) = 0, processed at reset. On the basis of the above mentioned specifications a LUT design is being proposed with the following key features:
• The encoder is used in designs that map L-bit inputs to (L-1)-bit LUT addresses.
• A 3 to 5 decoder is used which addresses the five memory locations.
• All the other multiples (even & odd) multiples of H are using a barrel shifter for producing the right shifts.
• A memory array of (2*L*/2) words is required which stores all the odd multiplies S in memory.
• A circuit (control circuit) is used to generate the control bits that are fed to the barrel shifter that does the required output shift.

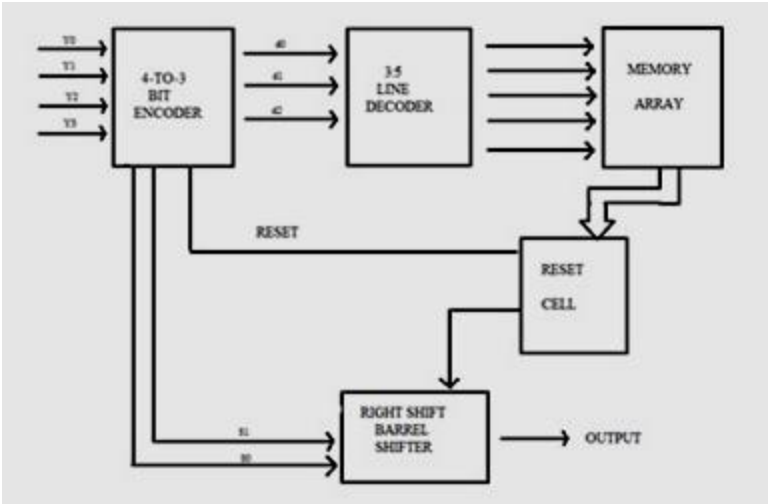

Fig 2: Proposed Efficient OMS-LUT Multiplier

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Initially, the precomputed product term containing zeros is stored in memory. The efficient OMS multiplier proposed for N = 4 is a memory array, a 4:3 line encoder, a 3:5 decoder and reset unit, a barrel shifter, and a control circuit, where N is the number of input words size. The control circuit generates the control bits for the two-stage barrel shifter.

Table 1: Truth Table for Efficient OMS Technique

Address $d_0d_1d_2$	Word symbol	Input $y_0y_1y_2y_3$	Shifts Required	Control circuit bits S1 S2
0 0 0	P0	0 0 0 1 1 0 0 0 0 1 0 0 0 0 1 0	0 1 2 3	0 0 0 1 1 0 1 1
0 0 1	P1	0 1 0 1 1 0 1 0	0 1	0 0 0 1
0 1 0	P2	1 0 0 1 1 1 0 0	0 1	0 0 0 1
		0 1 1 0	2	1 0
		0 0 1 1	3	1 1
0 1 1	P3	1 1 0 1 1 1 1 0	0 1	0 0 0 1
		0 1 1 1	2	1 0
		1 0 1 1	3	1 1
1 0 0	P4	1 1 1 1	0	0 0

Use 3:5 decoder to get 3-bit address from encoder and generate 5-word select signal. These five output lines from the decoder are used as addresses to retrieve the product term from memory.In Table 2, we see that 3 is the maximum number of shifts required, so a two-stage logarithmic barrel shifter is used to achieve the required right shift. Table 1 shows the number of shifts that must be performed on the LUT output and control bits S0 and S1 for different Y values.The input X=(0000) gives a product of zero which represents the multiplication of Zero. So, in this case the LUT is reset. A NOR cell consists of (W+4) NOR gates for the reset function, also known as a RESET cell with active-high RESET.

2. RESULTS

Many applications like that of signal processing and image processing using FIR digital filters [13]-[15] can be made using the proposed design, which is an efficient memory-based implementation that reduces power and complexity. Here, memory-based multiplication uses

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reduced-area LUT-based multipliers. We propose a LUT-based multiplier that mainly stores 1, 5, 9, 13, 15 entries (all odd entries) in memory. Multiply an M-bit fixed coefficient S by an unsigned 4-bit input. We implement a design-efficient OMS approach and compare existing storage approaches with existing OMS approaches. The Proposed scheme uses (3:5) decoder in comparison to the conventional OMS scheme which uses (3:8) decoder circuit. The software used to simulate the proposed efficient design was designed using Model-Sim Altera 6.4a software and Xilinx ISE Design Suite 14.5 for memory-based multiplication simulation and synthesis.Figures 3, 4 and 5 depict the schematic view of the proposed Efficient OMS design, the simulation results and the synthesis report of the design proposed in this paper.

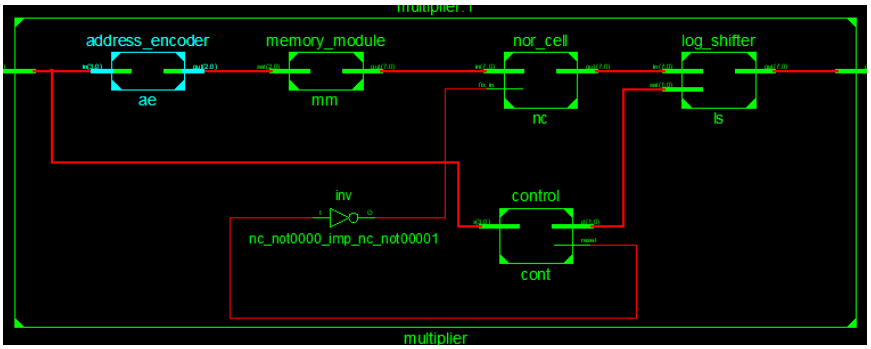

Fig 3: Schematic of the proposed design

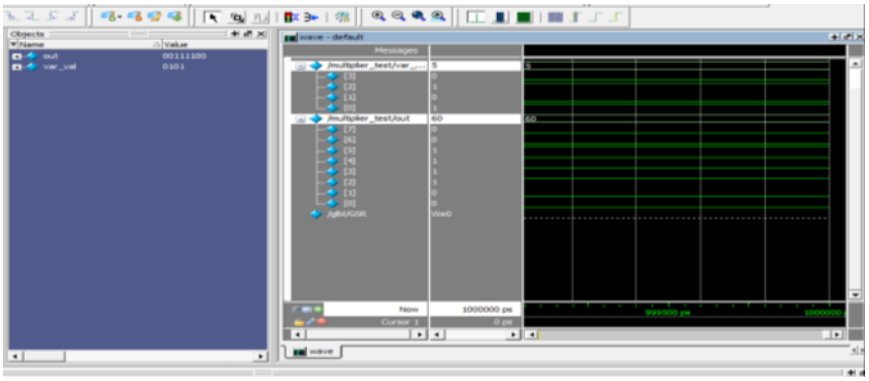
Fig 4: Simulation Results of the Proposed Design

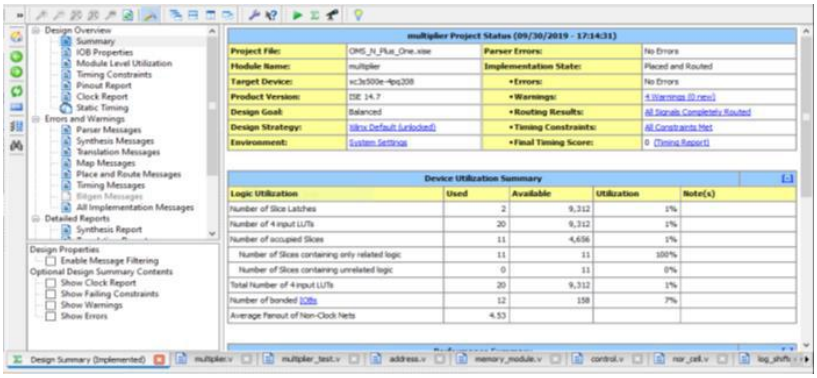
Fig 5: Synthesis Results of the proposed design

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Table 2: Comparison of Multipliers

Designs	**Conventional Multiplier**	**OMS- LUT-Multiplie r**	**Efficient OMS- LUT Multiplie r**
memory	[16×(M+4) ×N]-bit memory	[8×(M+4) ×N]-bit memory	[5×(M+4) ×N]-bit memory
Decoder used	(4:16 decoders)	(3:8 decoders)	(3:5 decoder)
Computational Path Delay	More	Less	Less
throughput	1 per cycle	1 per cycle	1 per cycle

3. CONCLUSIONS

An Efficient OMS technique for multiplication is presented in this paper which reduces the memory of LUT to a considerable amount when compared with the conventional technique and conventional OMS technique. The comparison of the multipliers is presented in Table 3 which shows that the Efficient OMS-LUT technique uses [5×(M+4)×N]-bit memory unit which is less in comparison to conventional and OMS design of LUT and provides more efficient computations. Thus memory-based multiplication techniques can be used in designing of various DSP circuit models which include FIR filter and adaptive filter design. Adaptive filter [11] design can be made successful if the coefficient of the multiplier is made variable and not fixed using various adaptive filter algorithms. Further optimizations can be made in this Efficient OMS design which reduces memory and area requirements, thus making an efficient design for VLSI-DSP computations.

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